THE INVENTION CLAIMED IS:

1. A method of manufacturing an integrated circuit comprising:
depositing a charge-trapping dielectric layer over a semiconductor substrate;
forming first and second bitlines in the semiconductor substrate;
5 forming a wordline over the charge-trapping dielectric layer; and
depositing a dielectric layer over the wordline wherein a structure selected from a group consisting of the charge-trapping dielectric layer, the wordline, the spacer, the interlayer dielectric layer, and a combination thereof is deuterated.

2. The method of manufacturing an integrated circuit as claimed in claim 1
10 wherein the depositing and forming include depositing deuterated materials for a structure selected from a group consisting of the charge-trapping dielectric layer, the wordline, the interlayer dielectric layer, and a combination thereof.

3. The method of manufacturing an integrated circuit as claimed in claim 1 including deuterating a structure selected from a group consisting of the charge-trapping
15 dielectric layer, the wordline, the interlayer dielectric layer, and a combination thereof.

4. The method of manufacturing an integrated circuit as claimed in claim 1 wherein depositing the charge-trapping layer, the wordline, and the interlayer dielectric layer deposits materials selected from a group consisting of a deuterated silicon oxide, a deuterated silicon nitride, a deuterated silicon oxynitride, a polysilicon, a glass, and a combination
20 thereof.

5. The method of manufacturing an integrated circuit as claimed in claim 1 wherein the depositing and forming use a process selected from a group consisting of high-density plasma deposition, rapid thermal chemical vapor deposition, low pressure chemical vapor deposition, rapid thermal oxidation, annealing in deuterium gas, and a combination
25 thereof.

6. A method of manufacturing an integrated circuit comprising:
depositing a first dielectric layer on a semiconductor substrate;
depositing a charge-trapping layer over the first dielectric layer;
depositing a second dielectric layer over the charge-trapping layer;
30 forming first and second bitlines in the semiconductor substrate;
forming a wordline over the second dielectric layer;
forming a spacer around the wordline; and

depositing an interlayer dielectric layer over the wordline wherein a structure selected from a group consisting of the first dielectric layer, the second dielectric layer, the wordline, the spacer, the interlayer dielectric layer, and a combination thereof is deuterated.

5 7. The method of manufacturing an integrated circuit as claimed in claim 6 wherein the depositing and forming include depositing deuterated materials for a structure selected from a group consisting of the first dielectric layer, the charge-trapping layer, the second dielectric layer, the wordline, the spacer, the interlayer dielectric layer, and a combination thereof.

10 8. The method of manufacturing an integrated circuit as claimed in claim 6 including deuterating a structure selected from a group consisting of the first dielectric layer, the charge-trapping layer, the second dielectric layer, the wordline, the spacer, the interlayer dielectric layer, and a combination thereof.

9. The method of manufacturing an integrated circuit as claimed in claim 6
15 wherein depositing the first dielectric layer, the charge-trapping layer, the second dielectric layer, the wordline, the spacer, and the interlayer dielectric layer deposits materials selected from a group consisting of deuterated silicon oxide, a deuterated silicon nitride, a deuterated silicon oxynitride, a polysilicon, a glass, and a combination thereof.

10. The method of manufacturing an integrated circuit as claimed in claim 1
20 wherein the depositing and forming use a process selected from a group consisting of high-density plasma deposition, rapid thermal chemical vapor deposition, low pressure chemical vapor deposition, rapid thermal oxidation, annealing in deuterium gas, and a combination thereof.

11. An integrated circuit comprising:
25 a semiconductor substrate;
a charge-trapping dielectric layer over the semiconductor substrate;
first and second bitlines in the semiconductor substrate;
a wordline over the charge-trapping dielectric layer; and
a dielectric layer over the wordlines wherein a structure selected from a group
30 consisting of the charge-trapping dielectric layer, the wordline, the interlayer dielectric layer, and a combination thereof contains deuterium.

12. The integrated circuit as claimed in claim 11 wherein for a structure selected from a group consisting of the charge-trapping dielectric layer, the wordline, the interlayer dielectric layer, and a combination thereof contains deuterium diffused from another structure selected from a group consisting of the charge-trapping dielectric layer, the wordline, the
5 interlayer dielectric layer, and a combination thereof.

13. The integrated circuit as claimed in claim 11 including the charge-trapping layer, the wordline, the spacer, and the interlayer dielectric layer are of materials selected from silicon oxide, silicon nitride, silicon oxynitride, polysilicon, glass, and a combination thereof.

10 14. The integrated circuit as claimed in claim 11 wherein the charge-trapping layer, the wordline, the spacer, and the interlayer dielectric layer are of materials selected from a deuterated silicon oxide, a deuterated silicon nitride, a deuterated silicon oxynitride, a deuterated polysilicon, a deuterated glass, and a combination thereof.

15. The integrated circuit as claimed in claim 11 including additional structures in
15 the integrated circuit containing deuterium.

16. An integrated circuit comprising:

a first dielectric layer on a semiconductor substrate;

a charge-trapping layer over the first dielectric layer;

a second dielectric layer over the charge-trapping layer;

20 first and second bitlines in the semiconductor substrate;

a wordline over the second dielectric layer;

a spacer around the wordline; and

an interlayer dielectric layer over the wordlines wherein a structure selected from a group consisting of the first dielectric layer, the second dielectric layer, the
25 wordline, the spacer, the interlayer dielectric layer, and a combination thereof contain deuterium.

17. The integrated circuit as claimed in claim 16 wherein a structure selected from a group consisting of the first dielectric layer, the charge-trapping layer, the second dielectric layer, the wordline, the spacer, the interlayer dielectric layer, and a combination thereof
30 contains deuterium diffused from another structure selected from a group consisting of the first dielectric layer, the charge-trapping layer, the second dielectric layer, the wordline, the spacer, the interlayer dielectric layer, and a combination thereof.

18. The integrated circuit as claimed in claim 16 wherein the first dielectric layer, the charge-trapping layer, the second dielectric layer, the wordline, the spacer, and the interlayer dielectric layer are of materials selected from silicon oxide, silicon nitride, silicon oxynitride, a polysilicon, glass, and a combination thereof.

5 19. The integrated circuit as claimed in claim 16 wherein the first dielectric layer, the charge-trapping layer, the second dielectric layer, the wordline, the spacer, and the interlayer dielectric layer are of materials selected from a deuterated silicon oxide, a deuterated silicon nitride, a deuterated silicon oxynitride, a deuterated polysilicon, a deuterated glass, and a combination thereof.

10 20. The integrated circuit as claimed in claim 16 including additional silicon structures in the integrated circuit containing deuterium.